SUPER LOW-NOISE SELF-ALIGNED GATE GaAs MESFET WITH NOISE FIGURE OF 0.87dB AT 12GHz

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ABSTRACT

Advanced self-aligned multi-layer gate FET (SAMFET) is developed for super low-noise MMIC amplifiers. Reduction of gate resistance by adopting a novel T-shaped multi-layer gate results in improvement of minimum noise figure by 0.2dB compared with conventional SAMFET. At 12GHz, advanced SAMFET gives a minimum noise figure of 0.87dB with associated gain of 10.62dB. Excellent uniformity of performances and high reliability are confirmed. They are owing to complete planer structure and refractory WSi gate contact. This technology is considered to be promising for high performance and low cost MMICs.

INTRODUCTION

Recently, demands for super low-noise amplifiers have rapidly increased in microwave consumer applications such as direct broadcasting satellite (DBS) receivers. At present, although discrete HEMTs and/or MESFETs are widely used for those amplifiers, MMICs are strongly required to reduce the size and cost and to improve the reliability of the amplifiers.

A lot of works have been performed in order to improve the low-noise performance of discrete HEMTs and MESFETs, and minimum noise figure (NFmin) of around 0.5dB at 18GHz for sub-quarter micron gate HEMTs[1][2] and 0.8dB at 16GHz for half micron gate MESFETs[3] have been reported. However, conventional HEMTs and MESFETs are not suitable for high yield and high performance MMICs, because of their relatively poor uniformity and reproducibility due to the recessed gate structures. On the other hand, self-aligned gate MESFETs (SAGFETs) are superior to the recessed gate FETs in uniformity and manufacturability owing to their planar structures, which have been demonstrated in GaAs LSIs[4]. However, SAGFETs used in GaAs digital ICs are also unsuitable for microwave operation mainly because of its high gate resistance.

Low resistance gate structures for planar FET have been investigated by several workers[5-7], and we have demonstrated that the self-aligned multi-layer gate FET (SAMFET) with buried p-layer lightly doped drain (BPLDD) structure has high potential for low-noise operation (NFmin=1.07dB at 12GHz) and is uniform enough for high yield MMICs[8][9]. Moreover, refractory WSi gate provides high reliability of FET[7][10]. Using SAMFET technology, a noise figure of 1.58dB with a gain of 29dB was already obtained at 12GHz for 4-stage amplifier MMIC[9]. However, more improvement of noise figure is desired for high performance and low cost microwave system.

In this paper, fabrication process and performance of advanced SAMFET, which improves NFmin by about 0.2dB compared with conventional one [9], are described.

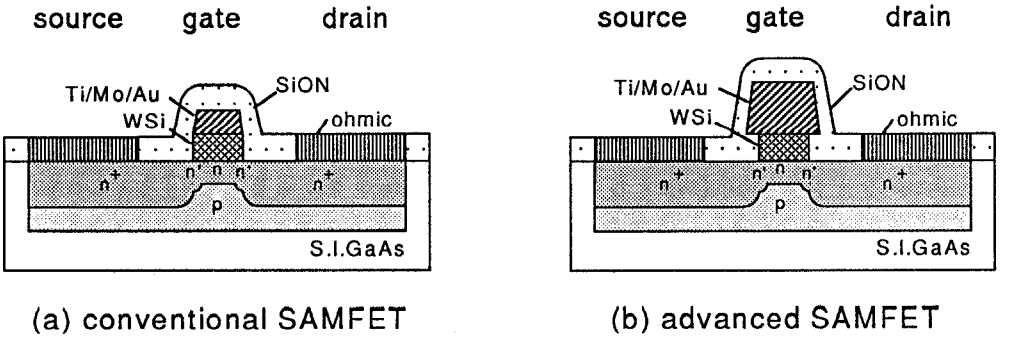

Fig.1 Schematic cross-sections of conventional SAMFET (a) and advanced SAMFET(b).

DEVICE AND PROCESS DESCRIPTION

Figure 1 (a) and (b) show schematic cross-sections of conventional SAMFET and advanced SAMFET, respectively. The difference is the structure of gate electrode. In case of conventional SAMFET, because the length of low resistance Au over-layer is same as that of WSi under-layer, the gate resistance is relatively high especially for sub-half micron gate, which limits improving low-noise performance. To obtain lower noise figure, the gate resistance must be reduced further. On this purpose, T-shaped gate is adopted to SAMFET.

Considering manufacturability, fabrication process without any additional photo masks is developed to realize T-shaped gate structure. Only five masks are required to fabricate advanced SAMFET. Figure 2 shows the fabrication process. The channel n-layer with buried p-layer is formed by selective ion-implantation into undoped semi-insulating (100) GaAs LEC substrate (a). Si and Mg are used for n- and p-layer, respectively. The buried p (BP)-layer is employed to suppress the short-channel effect. And BP-layer also increase transconductance as described below. To activate implanted ions, the substrate is annealed in a furnace at 800℃ for 30min with arsine atmosphere. WSi(0.3μm) and SiON(0.8μm) films are deposited by sputtering and plasma CVD, respectively. Then, T-shaped WSi/SiON pattern is delineated by RIE with 0.2μm WSi side-etching(b). So, the gate length of 0.4μm is obtained by using 0.8μm photo-resist mask. The gate length uniformity is good and its standard deviation is typically 0.03μm for 0.4μm gate.

The SiON over-layer acts as a mask for n^+-implantation and dummy gate to be replaced with low resistance metals. Oblique implantations (incident angle of ion beam is about 45°) are adopted to form n'-region under SiON overhangs(c). Then n^+-regions are formed by conventional implantation(d). The n' and n^+ implants are activated in the same manner of primary annealing. After planarization with photoresist(e), the SiON over-layer is replaced with 0.4μm thick Ti/Mo/Au layer by removing SiON with BHF solution, evaporation and lift-off(f). Finally, ohmic electrodes are formed using AuGe/Ni/Au and SiON film is deposited for passivation(g). All Photo-lithography is performed using stepper for high reproducibility.

The newly adopted techniques to realize the advanced SAMFET are WSi side-etching for T-shaped multi-layer gate and oblique ion-implantation for n'-region. Owing to the large cross section of Au over-layer, gate resistance is successfully reduced. The separation of n^+-region and gate electrode is effective to suppress the short-channel effect and to increase gate breakdown voltage. The n'-region contributes to lowering the series resistance without serious affection to short-channel effect and gate breakdown voltage, because both energy and dosage of n'-implantation are lower than those of n^+-implantation.

Figure 3 shows a cross sectional SEM photograph of advanced SAMFET after deposition of passivation film. The length of WSi under-layer which corresponds to gate length is 0.4μm as expected.

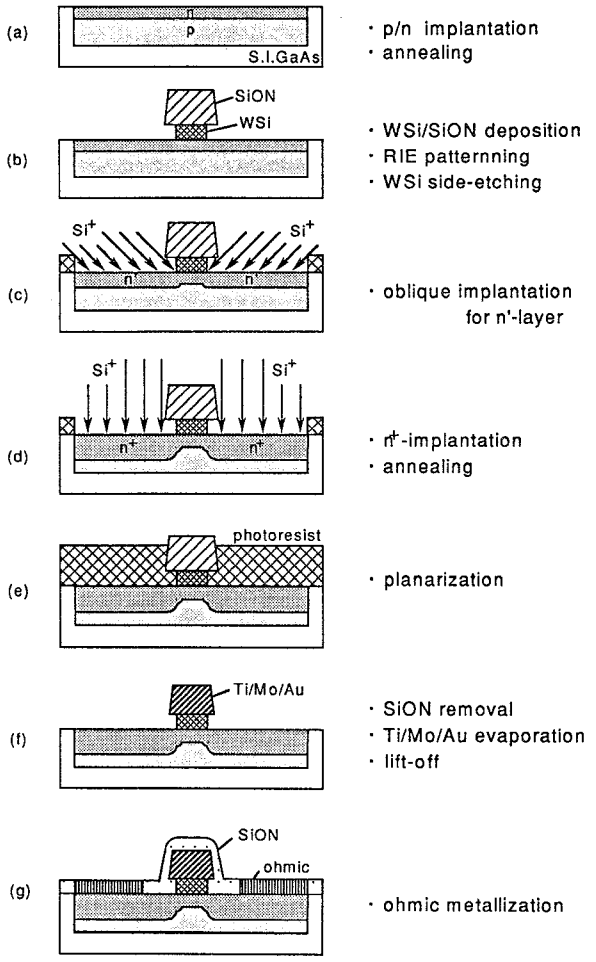

Fig.2 Fabrication process flow of advanced SAMFET.

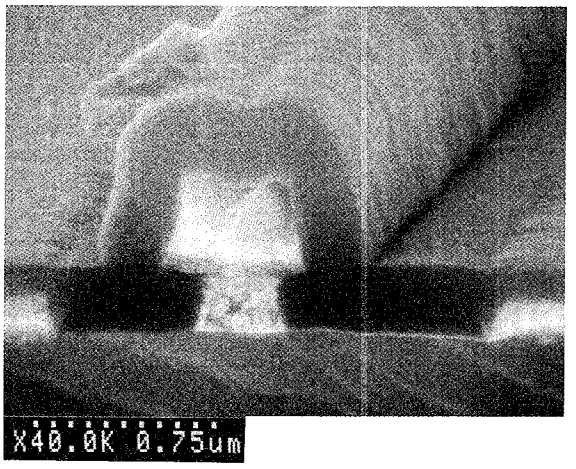

Fig.3 SEM photograph of advanced SAMFET.

DC AND MICROWAVE PERFORMANCES

Figure 4 shows a typical gate bias voltage (Vgs) dependence of transconductance (gm) and source-to-drain current (Ids) of 0.4μm gate advanced SAMFET. In this figure, gm of SAMFET without BP-layer is superimposed with dashed line for comparison. Improvement of gm and pinch-off characteristic owing to the BP-layer are apparent. This is account for by the thinning of the effective channel owing to the depletion layer of p-n junction. Maximum gm is as high as 370mS/mm and gm at Ids = 10mA is 260mS/mm. Using measured source resistance of 0.6 ohm·mm, maximum intrinsic gm of 480mS/mm is assumed. Gate breakdown voltage is typically 11V which is sufficient for low-noise applications.

RF measurement of advanced SAMFET having gate width of 75x2μm and gate length of 0.4μm is performed by on wafer probing in the frequency range from 0.2 to 40.2GHz. A current gain ($|H_{21}|$) is plotted in Fig.5 as a function of frequency. Cut off frequency (f_T) is estimated to be 40GHz. Standard deviation of f_T is as small as 1GHz over 3-inch substrate. Figure 6 shows the maximum stable and available gain (MSG/MAG) versus frequency. Advanced SAMFET is stable up to around 30GHz owing to the low gate resistance. MSGs of 12 and 8dB are obtained at 12 and 30GHz, respectively.

Figure 7 shows Ids dependence of NFmin and associated gain (Ga) at 12GHz. The lowest NFmin of 0.87dB with Ga of 10.62dB is obtained at Ids = 10mA This is 0.2dB lower than that of conventional SAMFET and is the best NFmin value of self-aligned gate MESFET ever reported. At 40GHz, the advanced SAMFET also shows very low NFmin of 2.18dB. The excellent low-noise performance is attributed to high transconductance and low gate resistance.

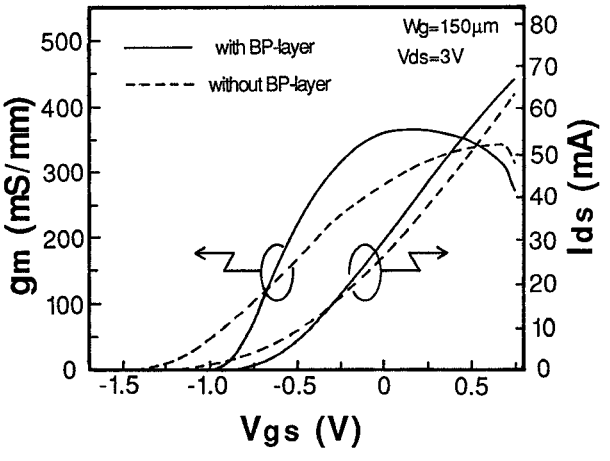

Fig.4 Vgs dependence of gm and Ids. Better pinch-off characteristics and higher gm are obtained for SAMFET with BP-layer.

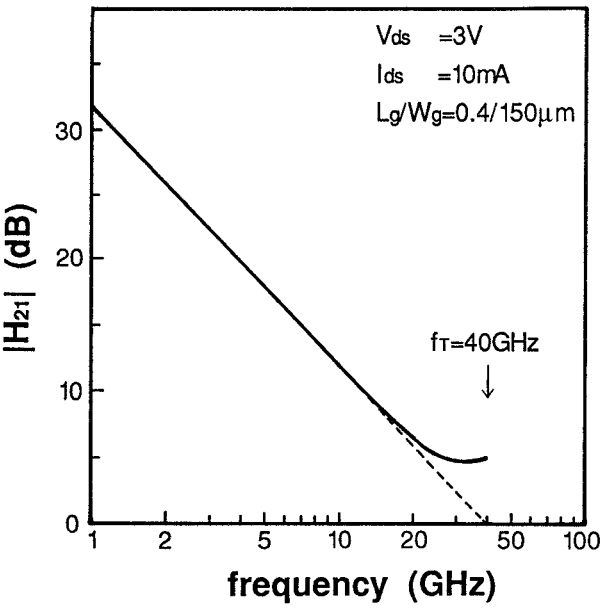

Fig.5 Frequency dependence of current gain |H21|. Estimated value of f_T is 40GHz.

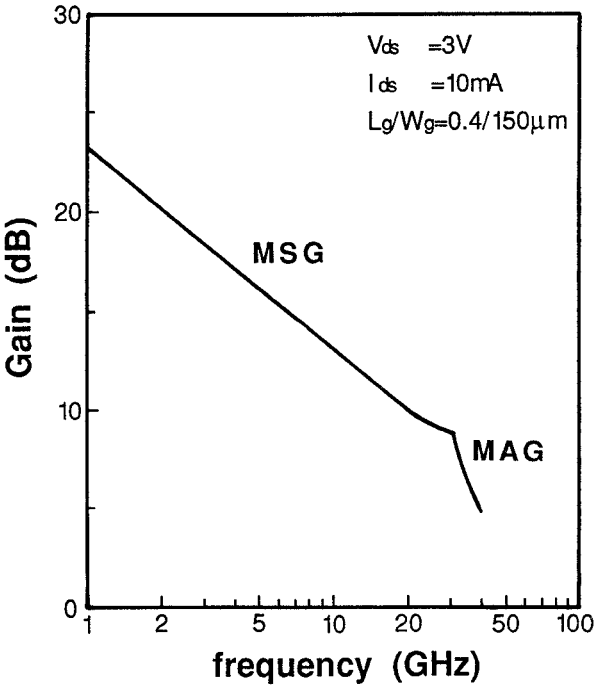

Fig.6 Frequency dependence of maximum stable and available gain . Advanced SAMFET is stable up to 30GHz.

Figure 8 shows NFmin distribution of the advanced SAMFET compared with the standard AlGaAs/GaAs HEMT having same gate length. SAMFET gives comparable NFmin in average and superior uniformity to HEMT. Standard deviations of NFmin are 0.08 and 0.15dB for SAMFET and HEMT, respectively. Owing to ion implanted planar structure, very high yield of 70% has been achieved for NFmin less than 1.0dB at 12GHz.

By high temperature DC biased test, it is also confirmed that SAMFET has high reliability. Under Tch = 180℃ and Vds = 5V, no remarkable degradation of NFmin and other parameters is observed for 1000hrs.

CONCLUSION

The advanced SAMFET with T-shaped multi-layer gate is very promising for super low-noise MMIC amplifiers from the view points of low-noise performance, uniformity, and reliability. NF min is improved by 0.2dB compared with conventional SAMFET as the result of gate resistance reduction. The best NFmin of 0.87dB with Ga of 10.62dB is obtained at 12GHz. Excellent uniformity of RF characteristics and noise performance and high reliability are also confirmed.

Using this technology, for example, noise figure of less than 1.3dB and gain of higher than 30dB can be expected for 4-stage MMIC amplifier at 12GHz. Furthermore, it is easy to realize analog and digital circuits integrated on a chip because the fabrication process of SAMFET is basically same as SAGFET.

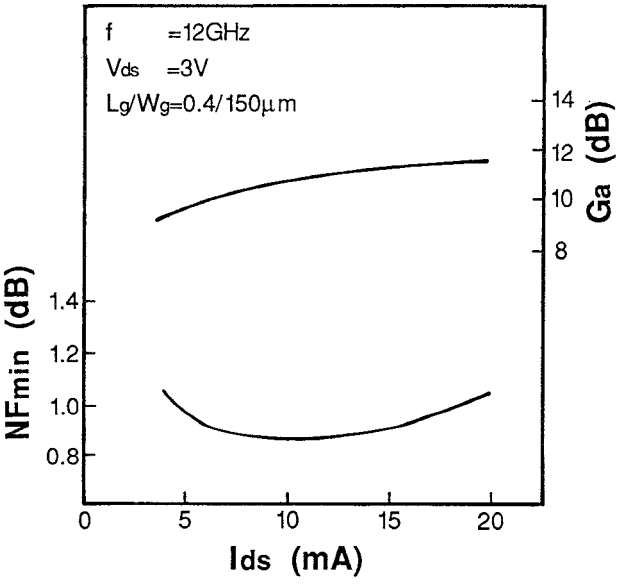

Fig.7 Ids dependence of NFmin and Ga. Minimum noise figure of 0.87dB with associated gain.

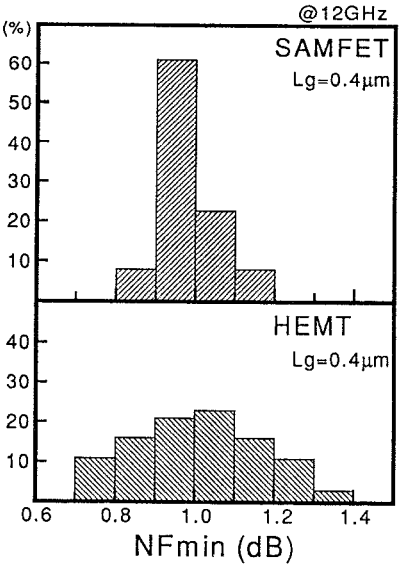

FIG 8. NF distribution of advanced SAMFET compared with standard HEMT having same gate length of 0.4um.

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